

OKI Semiconductor

MSC23840A-xxBS20/DS20

8,388,608-Word × 40-Bit DRAM MODULE : FAST PAGE MODE TYPE

DESCRIPTION

The OKI MSC23840A-xxBS20/DS20 is a fully decoded 8,388,608-word × 40-bit CMOS Dynamic Random Access Memory Module composed of twenty 16-Mb DRAMs (4M × 4) in SOJ packages mounted with twenty decoupling capacitors on a 72-pin glass epoxy single-inline package. This module is generally used for memory expansion in parity applications such as workstations.

FEATURES

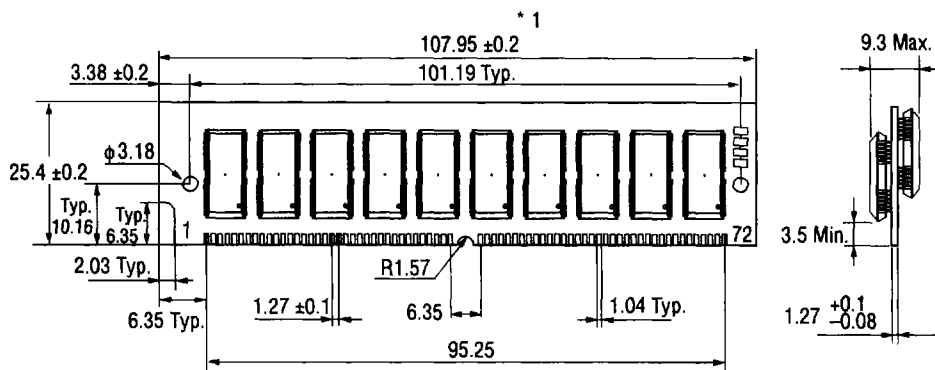
- 8-Meg × 40-bit organization
- 72-Pin Socket Insertable Module
 - MSC23840A-xxBS20 : Gold tab
 - MSC23840A-xxDS20 : Solder tab
- Single 5 V supply ±10% tolerance
- Access times : 60, 70, 80 ns
- Input : TTL compatible
- Output : TTL compatible, 3-state
- Refresh : 2048 cycles/32 ms
- CAS before RAS refresh, CAS before RAS hidden refresh, RAS-only refresh capability
- Multi-bit test mode capability
- Fast Page Mode capability

PRODUCT FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}		Operating (Max.)	Standby (Max.)
MSC23840A-60BS20/DS20	60 ns	30 ns	15 ns	110 ns	6875 mW	110 mW (MOS level)
MSC23840A-70BS20/DS20	70 ns	35 ns	20 ns	130 ns	6325 mW	
MSC23840A-80BS20/DS20	80 ns	40 ns	20 ns	150 ns	5775 mW	

PIN CONFIGURATION

MSC23840A-xxBS20/DS20



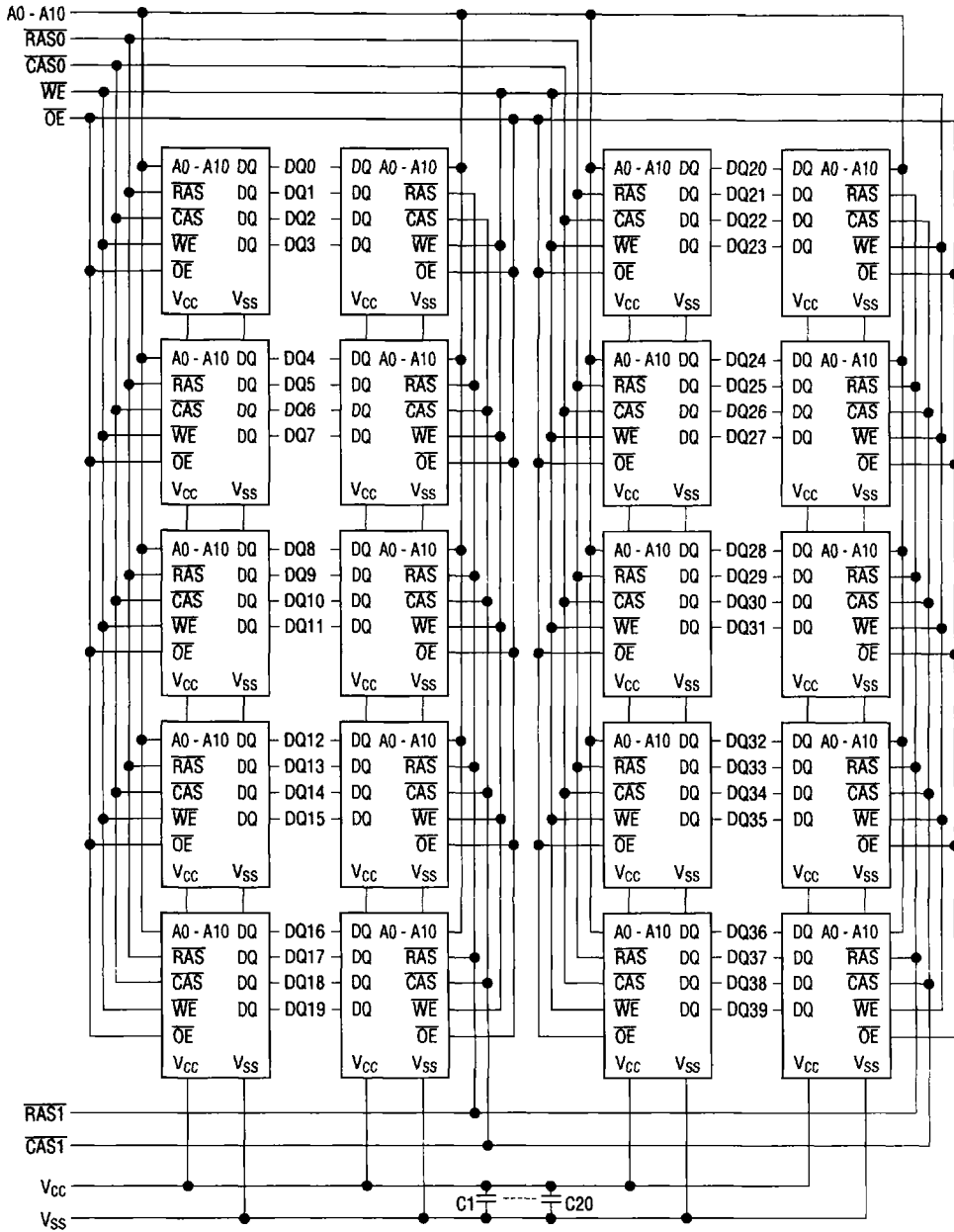
*1 The common size difference of the board width 12.5 mm of its height is specified as ±0.2. The value above 12.5 mm is specified as ±0.5.

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	16	A4	31	A8	46	DQ21	61	DQ33
2	DQ0	17	A5	32	A9	47	\overline{WE}	62	DQ34
3	DQ1	18	A6	33	NC	48	V _{SS}	63	DQ35
4	DQ2	19	\overline{OE}	34	NC	49	DQ22	64	DQ36
5	DQ3	20	DQ8	35	DQ17	50	DQ23	65	DQ37
6	DQ4	21	DQ9	36	DQ18	51	DQ24	66	DQ38
7	DQ5	22	DQ10	37	DQ19	52	DQ25	67	PD1
8	DQ6	23	DQ11	38	DQ20	53	DQ26	68	PD2
9	DQ7	24	DQ12	39	V _{SS}	54	DQ27	69	PD3
10	V _{CC}	25	DQ13	40	$\overline{CAS0}$	55	DQ28	70	PD4
11	PD5	26	DQ14	41	A10	56	DQ29	71	DQ39
12	A0	27	DQ15	42	NC	57	DQ30	72	V _{SS}
13	A1	28	A7	43	$\overline{CAS1}$	58	DQ31		
14	A2	29	DQ16	44	$\overline{RAS0}$	59	V _{CC}		
15	A3	30	V _{CC}	45	$\overline{RAS1}$	60	DQ32		

Presence Detect Pins

Pin No.	Pin Name	MSC23840A -60BS20/DS20	MSC23840A -70BS20/DS20	MSC23840A -80BS20/DS20
67	PD1	NC	NC	NC
68	PD2	V _{SS}	V _{SS}	V _{SS}
69	PD3	NC	V _{SS}	NC
70	PD4	NC	NC	V _{SS}
11	PD5	V _{SS}	V _{SS}	V _{SS}

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-1.0 to 7.0	V
Voltage V _{CC} Supply Relative to V _{SS}	V _{CC}	-1.0 to 7.0	V
Short Circuit Output Current	I _{OS}	50	mA
Power Dissipation	P _D	20	W
Operating Temperature	T _{opr}	0 to 70	°C
Storage Temperature	T _{stg}	-40 to 125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions(T_a = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	6.5	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

Capacitance(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A10)	C _{IN1}	—	135	pF
Input Capacitance (RAS0, RAS1, CAS0, CAS1)	C _{IN2}	—	80	pF
Input Capacitance (WE, OE)	C _{IN3}	—	155	pF
I/O Capacitance (DQ0 - DQ39)	C _{DQ}	—	26	pF

Note : Capacitance measured with Boonton Meter.

DC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0^\circ\text{C}$ to 70°C)

Parameter	Symbol	Condition	MSC23840A -60BS20/DS20		MSC23840A -70BS20/DS20		MSC23840A -80BS20/DS20		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
			Input Leakage Current	I_{LI}	$0\text{ V} \leq V_I \leq 6.5\text{ V}$; All other pins not under test = 0 V	-200	200	-200		
Output Leakage Current	I_{LO}	D_{OUT} disable $0\text{ V} \leq V_O \leq 5.5\text{ V}$	-20	20	-20	20	-20	20	μA	
Output High Voltage	V_{OH}	$I_{OH} = -5.0\text{ mA}$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	$I_{OL} = 4.2\text{ mA}$	0	0.4	0	0.4	0	0.4	V	
Average Power Supply Current (Operating)	I_{CC1}	\overline{RAS} , \overline{CAS} cycling, $t_{RC} = \text{Min.}$	—	1250	—	1150	—	1050	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	\overline{RAS} , $\overline{CAS} = V_{IH}$	—	40	—	40	—	40	mA	1
		\overline{RAS} , \overline{CAS} $\geq V_{CC} - 0.2\text{ V}$	—	20	—	20	—	20	mA	1
Average Power Supply Current (\overline{RAS} -only Refresh)	I_{CC3}	\overline{RAS} cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = \text{Min.}$	—	1250	—	1150	—	1050	mA	1, 2
Average Power Supply Current (\overline{CAS} before \overline{RAS} Refresh)	I_{CC6}	\overline{RAS} cycling, \overline{CAS} before \overline{RAS} , $t_{RC} = \text{Min.}$	—	1250	—	1150	—	1050	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS} = V_{IL}$, \overline{CAS} cycling, $t_{PC} = \text{Min.}$	—	1150	—	1050	—	950	mA	1, 3

- Notes: 1. Specified values are obtained with the output open.
 2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
 3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1,2,3,11,12

Parameter	Symbol	MSC23840A -60BS20/DS20		MSC23840A -70BS20/DS20		MSC23840A -80BS20/DS20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
		Random Read or Write Cycle Time	t _{RC}	110	—	130	—		
Read Modify Write Cycle Time	t _{RWC}	155	—	185	—	205	—	ns	
Fast Page Mode Cycle Time	t _{PC}	40	—	45	—	50	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{PRWC}	85	—	100	—	105	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	60	—	70	—	80	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	15	—	20	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	30	—	35	—	40	ns	4, 6
Access Time from $\overline{\text{OE}}$	t _{OE A}	—	15	—	20	—	20	ns	4
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	35	—	40	—	45	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	ns	4
Output Buffer Turn-off Delay Time	t _{OFF}	0	15	0	20	0	20	ns	7
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	15	0	20	0	20	ns	7
Transition Time	t _r	3	50	3	50	3	50	ns	3
Refresh Period	t _{REF}	—	32	—	32	—	32	ms	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15	—	20	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CP}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10K	20	10K	20	10K	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	45	20	50	20	60	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	15	40	ns	6
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	15	—	15	—	15	—	ns	
Column Address Hold Time from $\overline{\text{RAS}}$	t _{AR}	50	—	55	—	60	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	30	—	35	—	40	—	ns	

AC Characteristics (2/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1,2,3,11,12

Parameter	Symbol	MSC23840A -60BS20/DS20		MSC23840A -70BS20/DS20		MSC23840A -80BS20/DS20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
		Read Command Set-up Time	t _{RCS}	0	—	0	—		
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	8
Read Command Hold Time referenced to RAS	t _{RRH}	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	ns	9
Write Command Hold Time	t _{WCH}	10	—	15	—	15	—	ns	
Write Command Hold Time from RAS	t _{WCR}	45	—	55	—	60	—	ns	
Write Command Pulse Width	t _{WP}	10	—	10	—	10	—	ns	
OE Command Hold Time	t _{OEH}	15	—	20	—	20	—	ns	
Write Command to RAS Lead Time	t _{RWL}	15	—	20	—	20	—	ns	
Write Command to CAS Lead Time	t _{CWL}	15	—	20	—	20	—	ns	
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	ns	10
Data-in Hold Time	t _{DH}	15	—	15	—	15	—	ns	10
Data-in Hold Time from RAS	t _{DHR}	50	—	55	—	60	—	ns	
OE to Data-in Delay Time	t _{OEED}	15	—	20	—	20	—	ns	
CAS to WE Delay Time	t _{CWD}	40	—	50	—	50	—	ns	9
RAS to WE Delay Time	t _{RWD}	85	—	100	—	110	—	ns	9
Column Address to WE Delay Time	t _{AWD}	55	—	65	—	70	—	ns	9
CAS Precharge to WE Delay Time	t _{CPWD}	60	—	70	—	75	—	ns	9
CAS Active Delay Time from RAS Precharge	t _{RPC}	10	—	10	—	10	—	ns	
RAS to CAS Set-up Time (CAS before RAS)	t _{CSR}	10	—	10	—	10	—	ns	
RAS to CAS Hold Time (CAS before RAS)	t _{CHR}	20	—	20	—	20	—	ns	
CAS Precharge Time (Refresh Counter Test)	t _{CPT}	40	—	40	—	40	—	ns	
WE to RAS Precharge Time (CAS before RAS)	t _{WRP}	10	—	10	—	10	—	ns	
WE Hold Time from RAS (CAS before RAS)	t _{WRH}	10	—	10	—	10	—	ns	
RAS to WE Set-up Time (Test Mode)	t _{WTS}	10	—	10	—	10	—	ns	
RAS to WE Hold Time (Test Mode)	t _{WTH}	20	—	20	—	20	—	ns	

- Notes:
1. A start-up delay of 200 μ s is required after power-up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
When using the internal refresh counter, a minimum of eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ initialization cycles is required.
 2. AC measurement assume $t_T = 5$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times are measured between V_{IH} and V_{IL} .
 4. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA} .
 7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves an open circuit condition and are not referenced to output voltage levels.
 8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.) the cycle is an early write cycle and the data output pin will remain in a high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), the cycle is a read modify write cycle and the data output pin will contain data read from the selected cell. If neither conditions is satisfied, the data output logic state (at access time) is undefined.
 10. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle or a read modify write cycle.
 11. The test mode is initiated by performing a $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is an 8-bit parallel test function. CA10, CA1 and CA0 are not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{\text{RAS}}$ -only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.
 12. In a test mode read cycle, the access time parameters are delayed by 5 ns. The test mode parameters are obtained by adding 5 ns to the normal read cycle values.

See ADDENDUM F for AC Timing Waveforms